13.3 ” Full HD
High brightness color LCD module

SPECIFICATION

MODEL NAME: LMTAB133ZM11

Date: 2017 / 03 / 29

Customer Signature		
Customer		
Approved Date	**Approved By**	**Reviewed By**

Contents

1. HANDLING PRECAUTIONS

1) Since front polarizer is easily damaged, pay attention not to scratch it.
2) Be sure to turn off power supply when inserting or disconnecting from input connector.
3) Wipe off water drop immediately. Long contact with water may cause discoloration or spots.
4) When the panel surface is soiled, wipe it with absorbent cotton or other soft cloth.
5) Since the panel is made of glass, it may break or crack if dropped or bumped on hard surface.
6) Since CMOS LSI is used in this module, take care of static electricity and insure human earth when handling.
7) Do not open or modify the Module Assembly.
8) Do not press the reflector sheet at the back of the module to any directions.
9) At the insertion or removal of the Signal Interface Connector, be sure not to rotate nor tilt the Interface Connector of the TFT Module.
10) After installation of the TFT Module into an enclosure, do not twist nor bend the TFT Module even momentary. At designing the enclosure, it should be taken into consideration that no bending/twisting forces are applied to the TFT Module from outside. Otherwise the TFT Module may be damaged.

2. General Description

2.1, Overview

This specification is a 13.3” TFT Liquid Crystal Display module with LED Backlight unit and 30 pins eDP interface. This module supports 1920 x 1080 FHD mode and can display 16,777,216 colors.

LED driving board for backlight unit is not included.

2.2 Features

- Sunlight readable display, 1000nits by LED backlight.
- Wide viewing angle
- RoHS Compliance

2.3 Application

Industrial Application.

2.4 Display Specifications

Items	Unit	Specification
Screen Diagonal	inch	13.3
Active Area	mm	293.76 (H) x 165.24 (V)
Pixels H x V	pixels	1920 x3(RGB) x 1080
Pixels Pitch	um	152.9 (per one triad) x 152.9
Pixel Arrangement		RGB Vertical stripe
Display mode		Normally black
White luminance (center)	Cd/m^2	1000 (Typ.)
Contrast ratio		700 (Typ.)
Optical Response Time	msec	25 ms (Typ. on/off)
Normal Input Voltage Vcc	Volt	3.3
Power Consumption (Vcc Line + LED backlight)	Watt	12.15 (Vcc line=0.86; LED line=11.29 W)
Weight	Grams	TBD (max.)
Physical size	mm	304.4(H) x 177.6(V) x 3.9 (D) (Max.) (187.82 with PCBA for (V))
Electrical Interface		eDP
Support Colors		16.7 M colors (8 bit)
Surface Treatment		Anti-Glare, 3H
Temperature range Operating Storage	 ^0C ^0C	 -10 ~ 50 -20 ~ 60
RoHS Compliance		RoHS Compliance

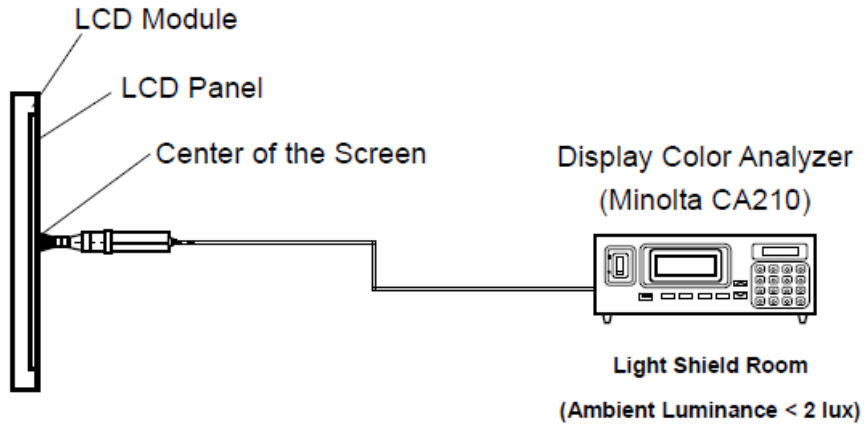
2.5 Optical Characteristics

The following optical characteristics are measured under stable condition at 25 ^{0}C

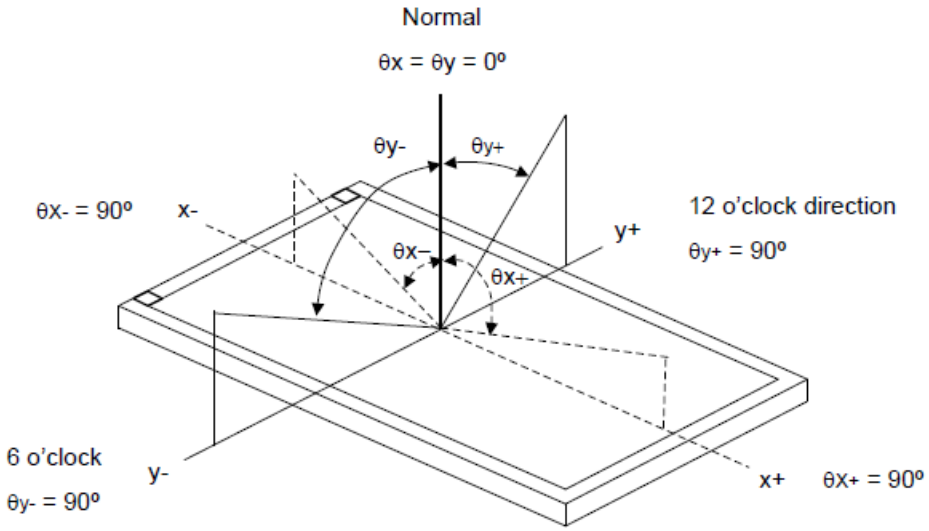
Items	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing angle	Deg.	Horizontal (Right) CR=10 (Left)	160	176		2
		Vertical (Up) CR=10 (Down)	160	176		
Contrast Ratio		Normal Direction	500	700		3
Response Time	msec	Raising time (T_{rR})		14		4
		Falling time (T_{rF})		11		
		Raising + Falling		25		
Color / Chromaticity Coordinates (CIE)		Red x	-0.05	0.64	+0.05	5
		Red y		0.34		
		Green x		0.31		
		Green y		0.61		
		Blue x		0.15		
		Blue y		0.07		
Color coordinates (CIE) White		White x		0.31		
		White y		0.34		
Center Luminance	Cd/m^2		800	1000		6
Luminance Uniformity	%		70	75		7
Crosstalk (in 60 Hz)	%				1.5	
Flicker	dB				-20	

Note 1: Measurement method

The LCD module should be stabilized at given temperature for 0.5 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



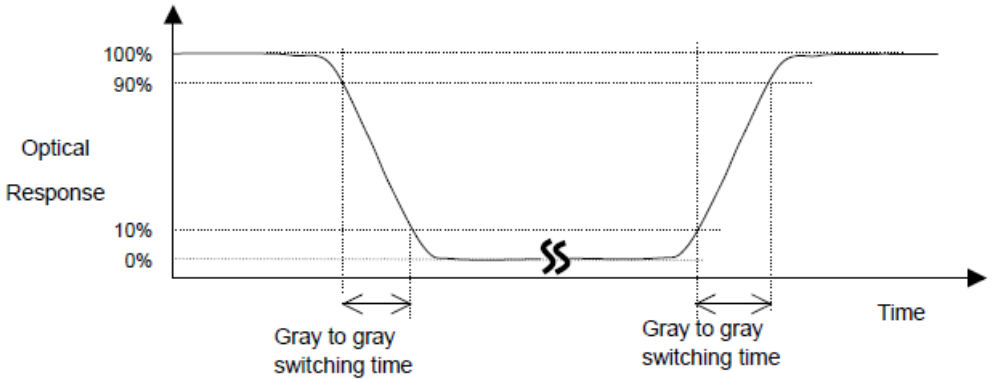
Note 2: Definition of viewing angle



Note 3: Contrast ratio is measured by Minolta CA210

Note 4: Definition of Response time

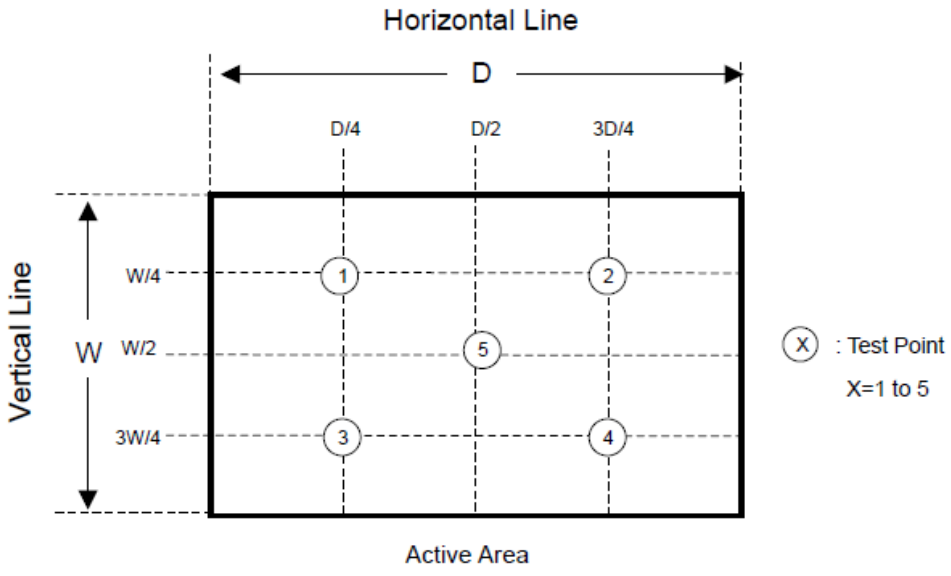
The output signals of photo detector are measured when the input signals are changed from “Full Black” to “Full White” (rising time), and from “Full White” to “Full Black” (falling time), respectively. The response time is interval between the 10% and 90% of amplitudes. Please refer to the figure as below.



Note 5: Color chromaticity and coordinates (CIE) is measured by Minolta CA210

Note 6: Center luminance is measured by Minolta CA210

Note 7: Luminance uniformity of these 5 points is defined as below and measured by Minolta CA210

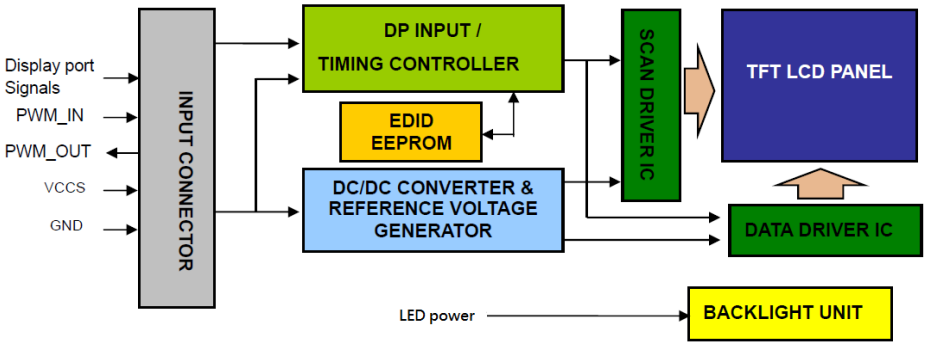


Uniformity = (Min. Luminance of 5 points) / (Max. Luminance of 5 points)

3. Functional Block Diagram

3.1 FUNCTION BLOCK DIAGRAM

The following diagram shows the functional block of the 13.3 inches Color TFT-LCD Module:

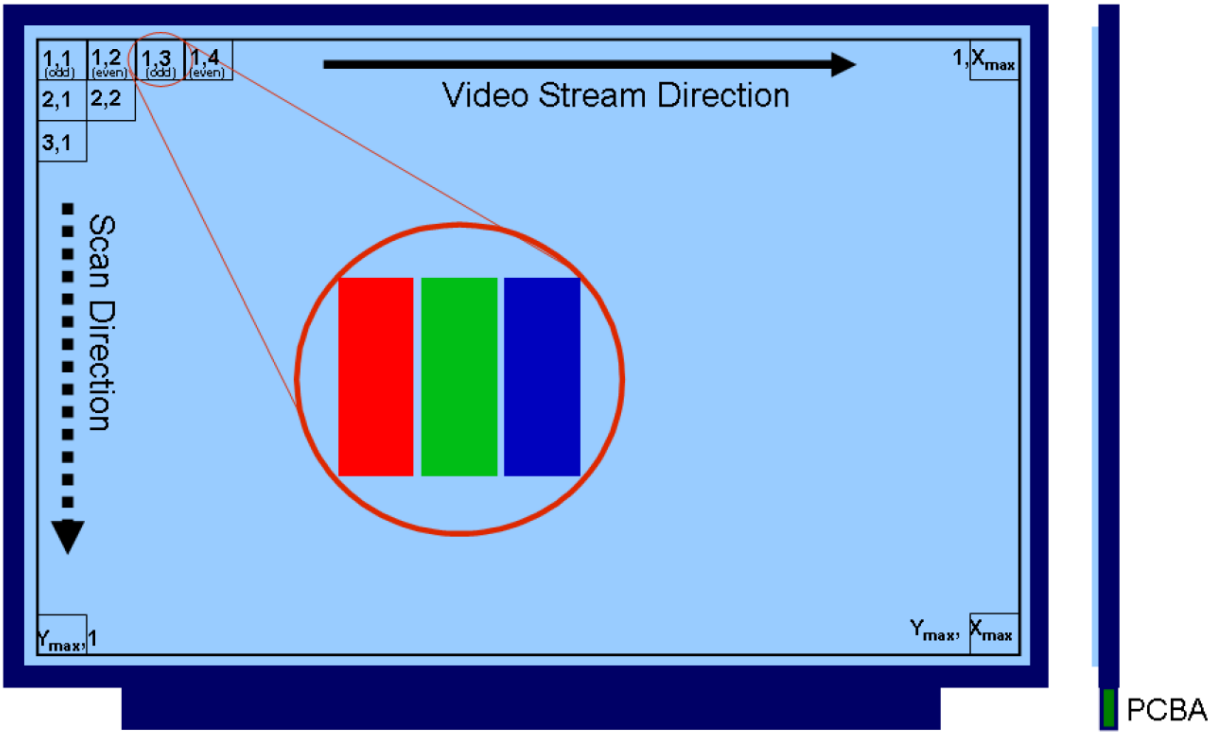


3.2 INTERFACE CONNECTIONS

PIN ASSIGNMENT

Pin	Symbol	Description	Remark
1	NC	No Connection (Reserved for LCD test)	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3 V (typical)	
13	VCCS	Power Supply +3.3 V (typical)	
14	BIST	Panel self test	
15	VSS	Ground	
16	HPD	Hot Plug Detect	
17	PWM_IN	System PWM signal input for dimming	
18	NC	No Connection (Reserved for LCD test)	
19	PWM_OUT	Panel PWM signal output to system	
20	NC	No Connection (Reserve)	
21	LED-	LED Cathode	
22	LED-	LED Cathode	
23	LED-	LED Cathode	
24	LED-	LED Cathode	
25	NC	No Connection (Reserve)	
Pin	Symbol	Description	Remark
26	LED+	LED Anode	
27	LED+	LED Anode	
28	NC	No Connection (Reserve)	
29	CLKDVCOM	D-Vcom Clock	
30	DATAVCOM	D-Vcom Data	

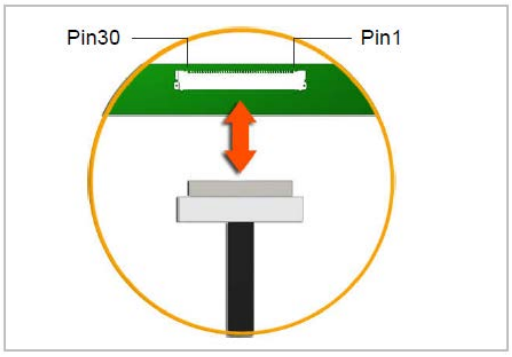
Note (1) The first pixel is odd as shown in the following figure.



Note (2) The I2C device addresses are defined as follows. The D-VCOM part is iML7978CL.

Component	Device Address							
	B7	B6	B5	B4	B3	B2	B1	WR
D-VCOM	1	0	0	1	1	1	1	X

CONNECTOR TYPE



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: IPEX-20455-030E-12

User's connector Part No: IPEX-20453-030T-01

4. Absolute Maximum Ratings

Absolute maximum ratings of the module are as following:

4.1 TFT LCD Module

Items	Symbol	Min	Max	Unit	Conditions
Power supply voltage	Vccs	-0.3	4.0	Volt	
Logic input voltage	Vin	-0.3	Vccs+0.3	Volt	

4.2 Backlight unit

Items	Symbol	Min	Max	Unit	Conditions
LED Current	I LED	--	480	mA	Note 1, 2

4.3 Absolute Ratings of Environment

Items	Symbol	Values			Unit	Conditions
		Min.	Typ.	Max.		
Operation temperature	T_{OP}	-10	-	50	^{0}C	Note 3
Operation Humidity	H_{OP}	5		90	%	
Storage temperature	T_{ST}	-20		60	^{0}C	
Storage Humidity	H_{ST}	5		90	%	

Note 1: With in Ta= 25℃

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to IIS (Incoming Inspection Standard).

5. Electrical characteristics

5.1 TFT LCD Module Power Specification

Input power specifications are as follows

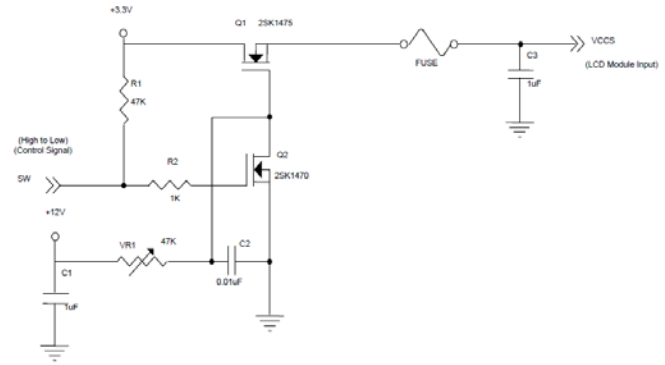
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCCS	3.0	3.3	3.6	V	(1)
HPD Impedance		R_{HPD}	30K			ohm	(4)
HPD		High Level	3.0	-	3.6	V	(5)
		Low Level	0	-	0.4	V	(5)
Ripple Voltage		V_{RP}	-	50	-	mV	(1)
PWM Input Voltage	High Level	V_{IHPWM}	2.3	-	3.6	V	
	Low Level	V_{ILPWM}	0	-	0.4	V	
PWM Control Duty Ratio			5		100	%	
PWM Input Frequency		f_{PWM}	190	-	2K	Hz	
PWMO Output Voltage	High Level	V_{OHPWMO}	2.0	-	3.6	V	
	Low Level	V_{OLPWMO}	0	-	0.8	V	
PWM Output Frequency		f_{PWM}	190	-	2K	Hz	
Inrush Current		I_{RUSH}	-	-	1.5	A	(1),(2)
Power Supply Current	Mosaic	Icc	-	315	375	mA	(3)a
	White		-	352	412	mA	(3)b

Note (1) The ambient temperature is Ta = 25 ± 2 ºC.

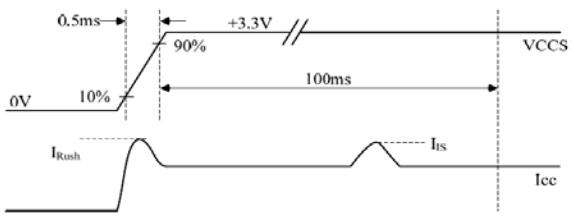
Note (2) IRUSH: the maximum current when VCCS is rising

I_{IS}: the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: white.:

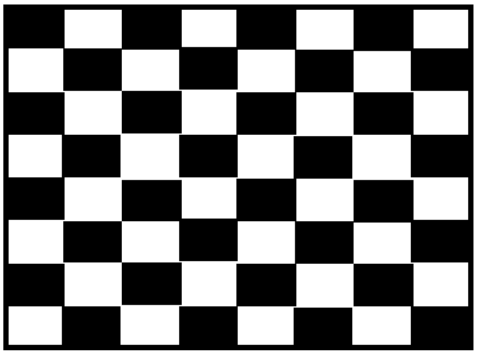


VCCS rising time is 0.5ms



Note (3) The specified power supply current is under the conditions at VCCS = 3.3 V, Ta = 25 ± 2 ºC, DC Current and fv = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. Mosaic Pattern



Active Area

b. White Pattern

Active Area

5.2 Backlight Unit

Parameter guideline is under stable conditions at 25℃ (Room Temperature):

Parameter	Min	Typ	Max	Unit	Note
LED voltage (VL)		29.7		[V]	2
LED current (IL)		380		[mA]	2,
LED Power (PL)		11.29		[W]	
LED Life Time(LTLED)		30,000		[Hour]	1

Note 1: The “LED lift time” is defined as the module brightness decrease to 50% original brightness that the ambient temperature is 25℃ and typical LED Current at 380 mA.

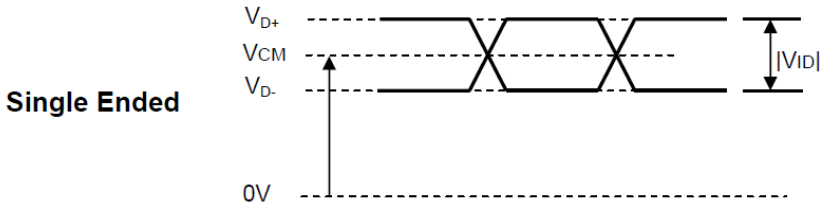
Note 2: PL=VL x IL x 1

5.3 DISPLAY PORT SIGNAL TIMING SPECIFICATION

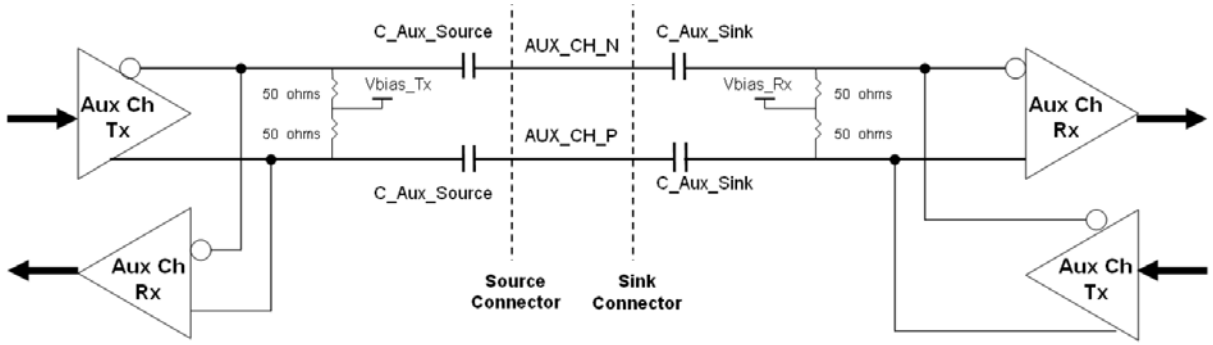
DISPLAY PORT INTERFACE

Parameter	Symbol	Min	Typ	Max	Unit	Note
Differential Signal Common Mode Voltage (MainLink and AUX)	VCM	0		2	V	(1)(3)
AUX AC Coupling Capacitor	C_{AUX}	75		200	nF	(2)
Main Link AC Coupling Capacitor	C_{MIL}	75		200	nF	(3)

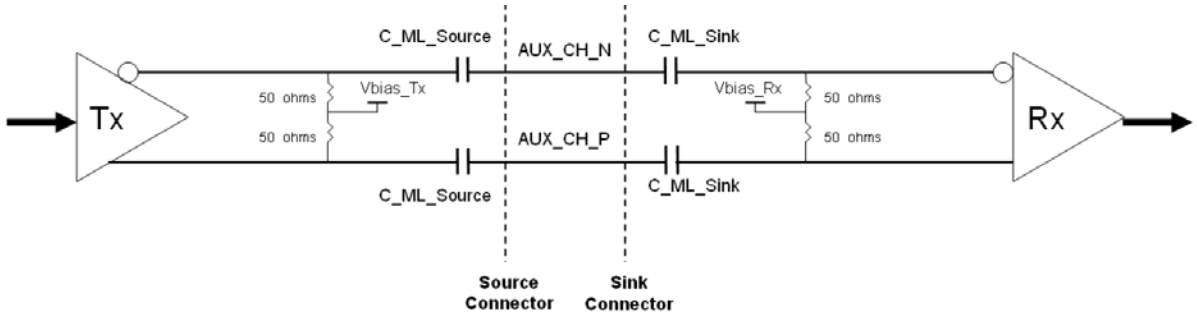
Note (1) Display port interface related AC coupled signals should follow VESA DisplayPort Standard Version1. Revision 1a and VESA Embedded DisplayPortTM Standard Version 1.1.



(2) Recommended eDP AUX Channel topology is as below and the AUX AC Coupling Capacitor (C_Aux_Source) should be placed on the source device.



(3) Recommended Main Link Channel topology is as below and the Main Link AC Coupling Capacitor (C_ML_Source) should be placed on the source device.



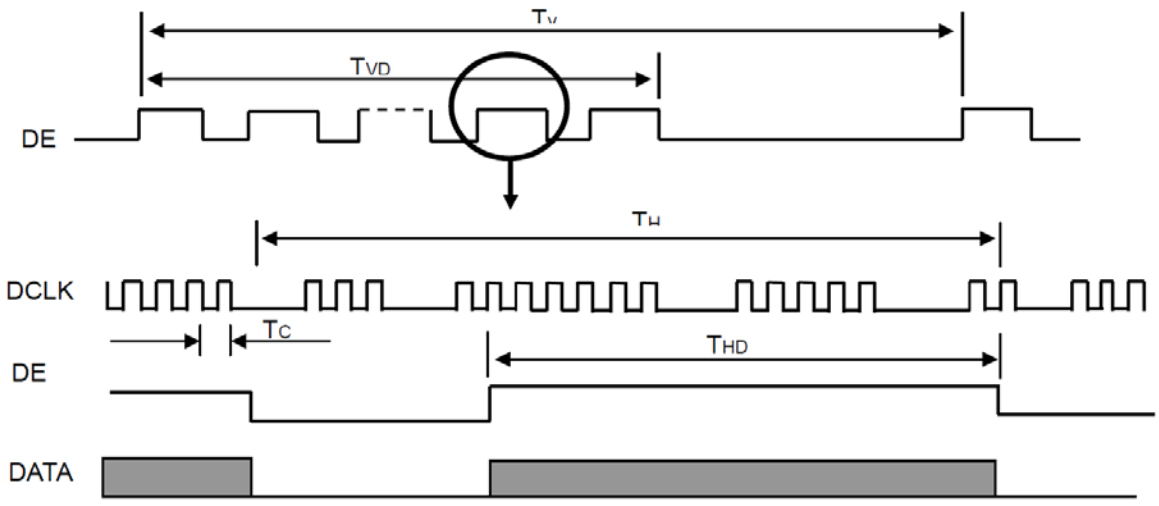
(4) The source device should pass the test criteria described in DisplayPortCompliance Test Specification (CTS) 1.1

5.4 DISPLAY TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

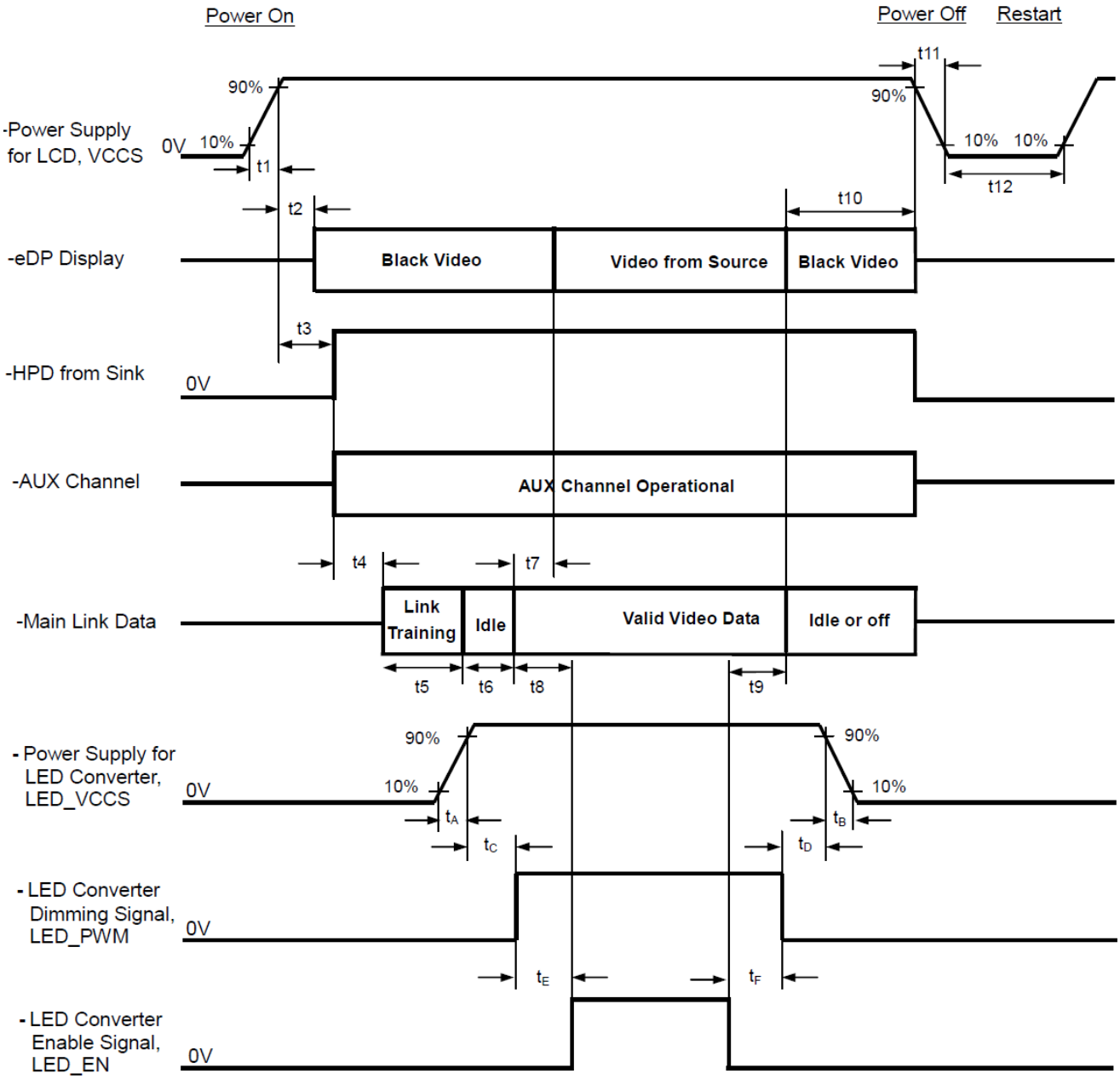
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	116.17	138.78	142.77	MHz	-
DE	Vertical Total Time	TV	1103	1112	1462	TH	-
	Vertical Active Display Period	TVD	1080	1080	1080	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	32	TV-TVD	TH	-
	Horizontal Total Time	TH	2058	2080	2910	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	TH-TH)	160	TH-THD	Tc	-
Frame Rate		--	--	60		--	-

INPUT SIGNAL TIMING DIAGRAM



5.5 Power ON/OFF Sequence

To prevent a latch-up or DC operation of LCD assembly, the power on/off sequence should be as the diagram below.



Timing Specifications: Follow VESA Embedded Display Port Standard Version 1

Parameter	Description	Reqd. By	Value		Unit	Notes
			Min	Max		
t1	Power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t2	Delay from LCD,VCCS to black video generation	Sink	0	200	ms	Automatic Black Video generation prevents display noise until valid video data is received from the Source (see Notes:2 and 3 below)
t3	Delay from LCD,VCCS to HPD high	Sink	0	200	ms	Sink AUX Channel must be operational upon HPD high (see Note:4 below)
t4	Delay from HPD high to link training initialization	Source	-	-	ms	Allows for Source to read Link capability and initialize
t5	Link training duration	Source	-	-	ms	Dependant on Source link training protocol
t6	Link idle	Source	-	-	ms	Min Accounts for required BS-Idle pattern. Max allows for Source frame synchronization
t7	Delay from valid video data from Source to video on display	Sink	0	50	ms	Max value allows for Sink to validate video data and timing. At the end of T7, Sink will indicate the detection of valid video data by setting the SINK_STATUS bit to logic 1 (DPCD 00205h, bit 0), and Sink will no longer generate automatic Black Video
t8	Delay from valid video data from Source to backlight on	Source	-	-	ms	Source must assure display video is stable
t9	Delay from backlight off to end of valid video data	Source	-	-	ms	Source must assure backlight is no longer illuminated. At the end of T9, Sink will indicate the detection of no valid video data by setting the SINK_STATUS bit to logic 0 (DPCD 00205h, bit 0), and Sink will automatically display Black Video. (See Notes: 2 and 3 below)
t10	Delay from end of valid video data from Source to power off	Source	0	500	ms	Black video will be displayed after receiving idle or off signals from Source
t11	VCCS power rail fall time, 90% to 10%	Source	0.5	10	ms	-
t12	VCCS Power off time	Source	500	-	ms	-
t_A	LED power rail rise time, 10% to 90%	Source	0.5	10	ms	-
t_B	LED power rail fall time, 90% to 10%	Source	0	10	ms	-

t_C	Delay from LED power rising to LED dimming signal	Source	1	-	ms	-
t_D	Delay from LED dimming signal to LED power falling	Source	1	-	ms	-
t_E	Delay from LED dimming signal to LED enable signal	Source	1	-	ms	-
t_F	Delay from LED enable signal to LED dimming signal	Source	1	-	ms	-

Note (1) Please don't plug or unplug the interface cable when system is turned on.

Note (2) The Sink must include the ability to automatically generate Black Video autonomously. The Sink must automatically enable Black Video under the following conditions:

- Upon LCDVCC power-on (within T2 max)
- When the "NoVideoStream_Flag" (VB-ID Bit 3) is received from the Source (at the end of T9)

Note (3) The Sink may implement the ability to disable the automatic Black Video function, as described in Note (2), above, for system development and debugging purposes.

Note (4) The Sink must support AUX Channel polling by the Source immediately following LCDVCC power-on without causing damage to the Sink device (the Source can re-try if the Sink is not ready). The Sink must be able to response to an AUX Channel transaction with the time specified within T3 max.

6. Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 60℃, 90%RH, 240hours	
High Temperature Operation (HTO)	Ta= 50℃, 50%RH, 240hours	3
Low Temperature Operation (LTO)	Ta= -10℃, 240hours	
High Temperature Storage (HTS)	Ta= 60℃, 240hours	
Low Temperature Storage (LTS)	Ta= -20℃, 240hours	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20℃/30min, 80℃/30min, 100 cycles	
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω) 1sec, 9 points, 25 times/ point.	
	Air Discharge: ± 15KV, 150pF(330Ω) 1sec 9 points, 25 times/ point.	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20℃ to 60℃, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

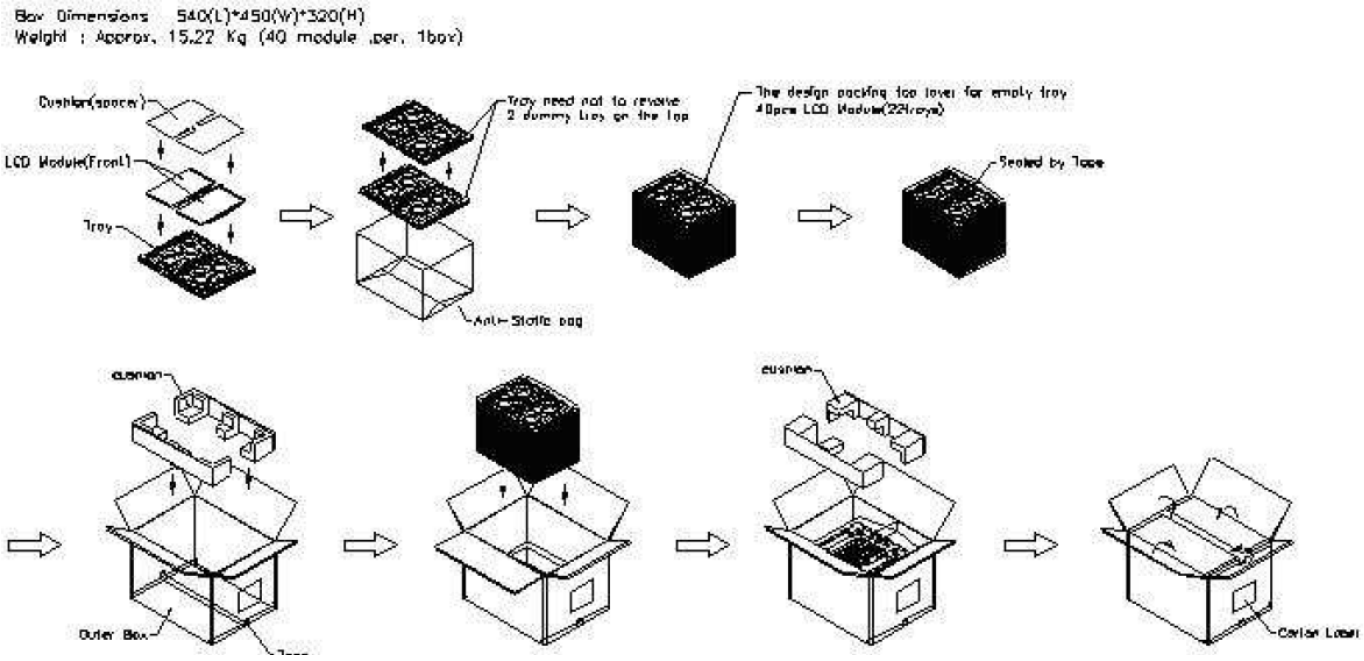
Note 3: The test items are tested by open frame type chassis.

7. Shipping Label & Package (TBD, Reference only)

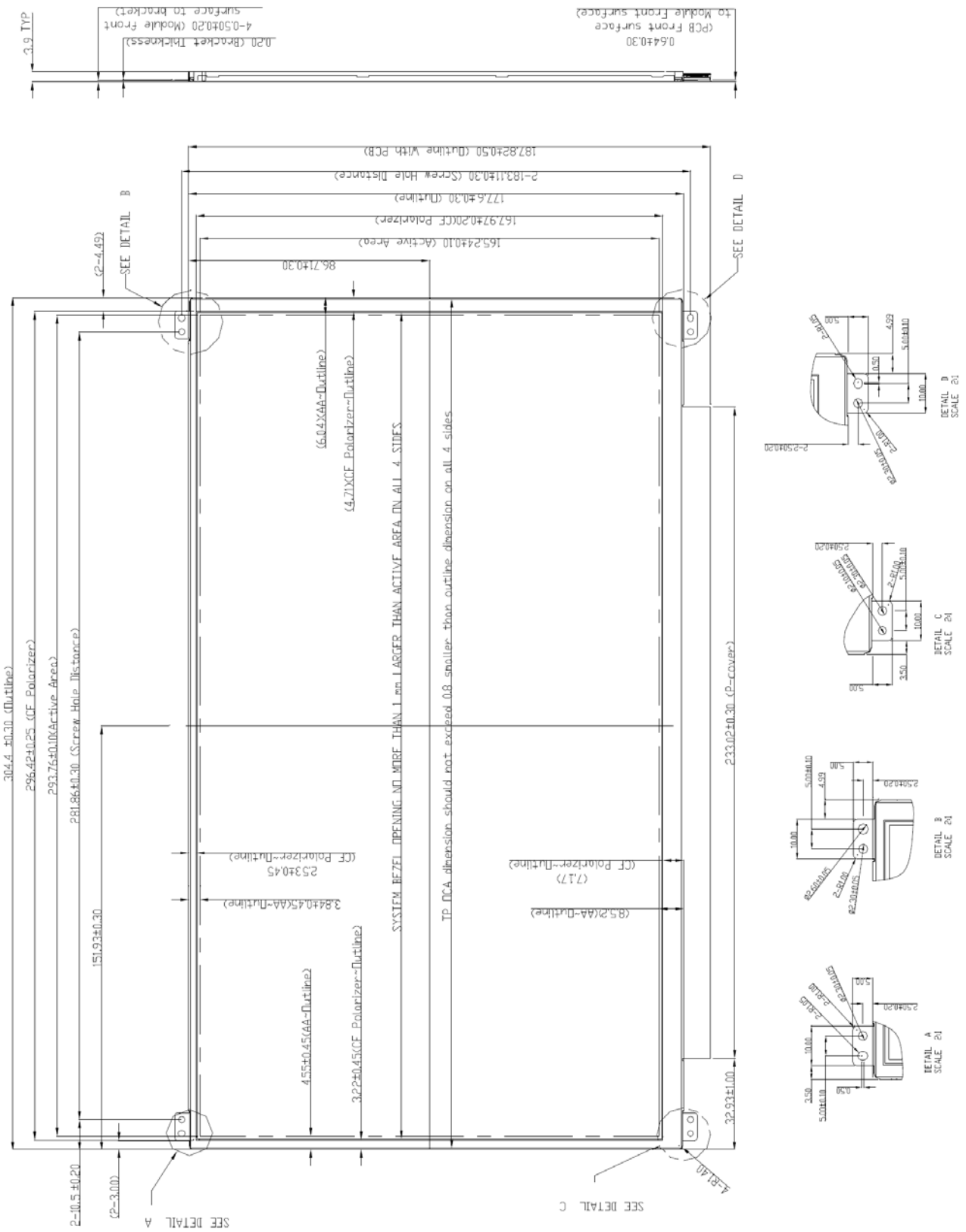
(1) 40pcs LCD modules / 1 Box

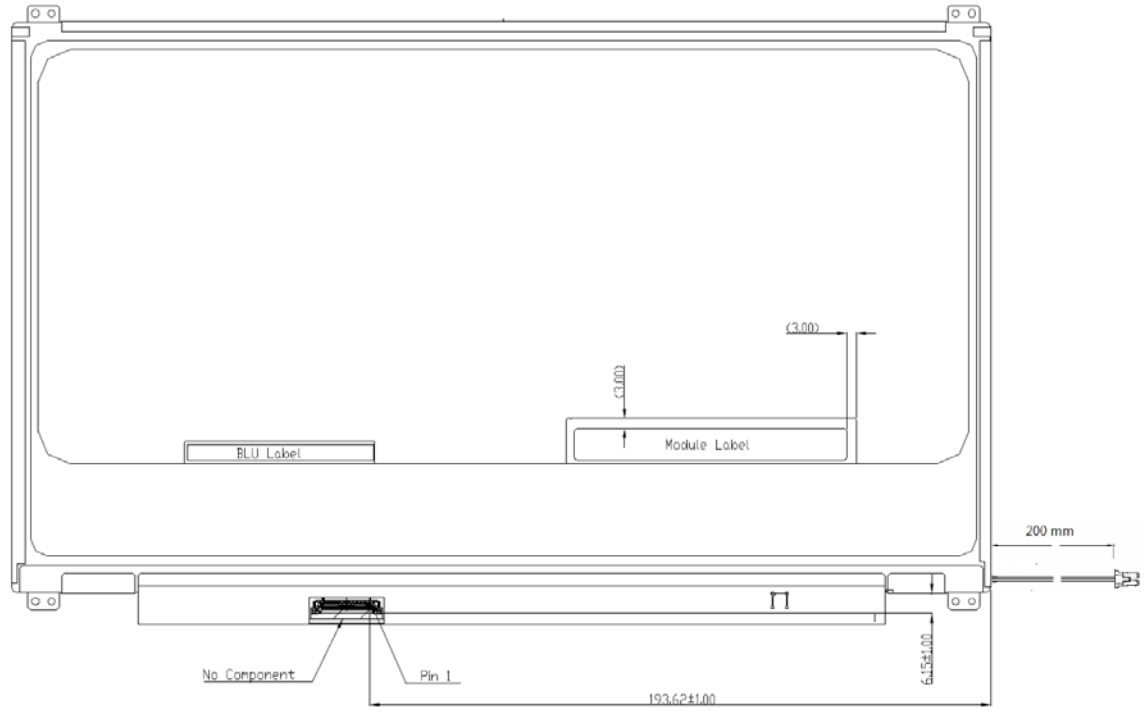
(2) Box dimensions: 540(L)x450(W)x320(H)mm

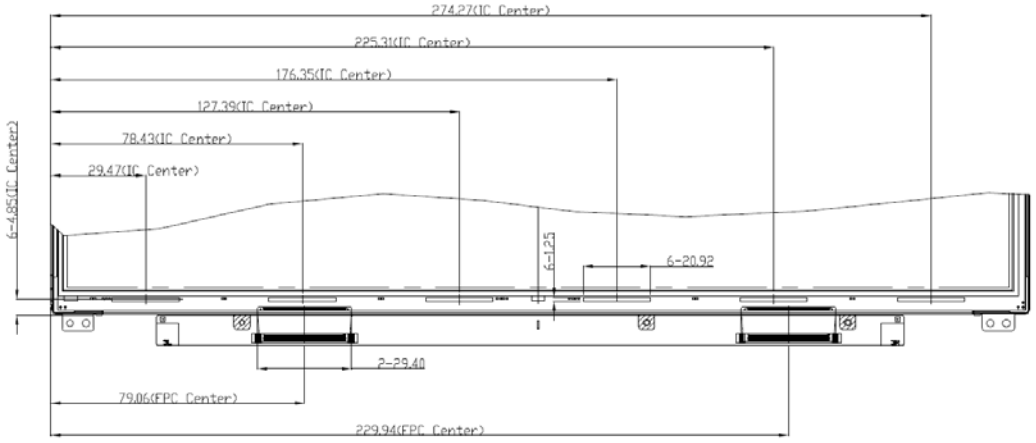
(3) Weight: TBD

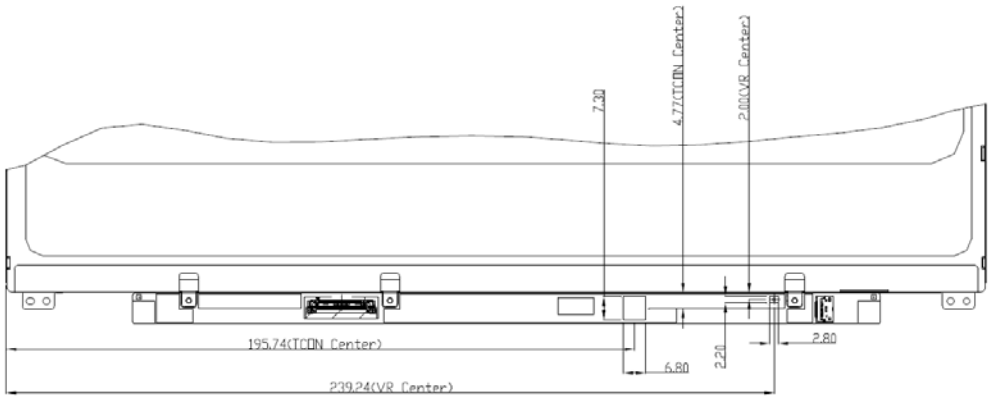


8. Mechanical Characteristic (mm)









NOTES :
1. LCD MODULE INPUT CONNECTOR : I-PEX 20455-030E-12.
2. IN ORDER TO AVOID ABNORMAL DISPLAY, POOLING AND WHITE SPOT,
   NO OVERLAPPING IS SUGGESTED AT CABLES, ANTENNAS, CAMERA, WLAN, WAN OR
   FOREIGN OBJECTS OVER FPC, T-CON AND VR LOCATIONS.
3. EDP CONNECTOR IS MEASURED AT PIN1 AND ITS MATING LINE.
4. MODULE FLATNESS SPEC 0.5mm MAX.
5. "( )" MARKS THE REFERENCE DIMENSIONS.

9. PRECAUTIONS

9.1 HANDLING PRECAUTIONS

(1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9) Do not disassemble the module.

(10) Do not pull or fold the LED wire.

(11) Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3) It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1) Do not pull the I/F connector in or out while the module is operating.

(2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

Appendix. EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPDI standards.

Byte # (decimal)	Byte # (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	00	Header	00	00000000
1	01	Header	FF	11111111
2	02	Header	FF	11111111
3	03	Header	FF	11111111
4	04	Header	FF	11111111
5	05	Header	FF	11111111
6	06	Header	FF	11111111
7	07	Header	00	00000000
8	08	ID system manufacturer name ("CMN")	0D	00001101
9	09	ID system manufacturer name	AE	10101110
10	0A	ID system Product Code (LSB)	45	01000101
11	0B	ID system Product Code (MSB)	13	00010011
12	0C	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
13	0D	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
14	0E	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
15	0F	32-bit serial # Unused(01h for VESA, 00h for SPWG)	00	00000000
16	10	Week of manufacture (fixed week code)	15	00010101
17	11	Year of manufacture (fixed year code)	16	00010110
18	12	Version=1	01	00000001
19	13	Revision=4	04	00000100
20	14	Vedio Input Definition	A5	10100101
21	15	Active area horizontal (“29.376cm“)	1D	00011101
22	16	Active area vertical (“16.524cm“)	11	00010001
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("RGB, Non-continous")	02	00000010
25	19	Rx1, Rx0, Ry1, Ry0, Gx1, Gx0, Gy1, Gy0	F1	11110001
26	1A	Bx1, Bx0, By1, By0, Wx1, Wx0, Wy1, Wy0	C6	11000110
27	1B	Rx=0.644	A4	10100100
28	1C	Ry=0.323	52	01010010
29	1D	Gx=0.270	45	01000101
30	1E	Gy=0.583	95	10010101
31	1F	Bx=0.144	24	00100100
32	20	By=0.109	1C	00011100
33	21	Wx=0.321	52	01010010
34	22	Wy=0.350	59	01011001
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1920x1080@40Hz)	00	00000000
37	25	No manufacturer's specific timing	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001

42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001
44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock (“138.78MHz”, According to VESA CVT Rev1.4)	36	00110110
55	37	# 1 Pixel clock (hex LSB first)	36	00110110
56	38	# 1 H active (“1920”)	80	10000000
57	39	# 1 H blank (“160”)	A0	10100000
58	3A	# 1 H active : H blank (“1920 :160”)	70	01110000
59	3B	# 1 V active (”1080”)	38	00111000
60	3C	# 1 V blank (”32”)	20	00100000
61	3D	# 1 V active : V blank (”1080 :32”)	40	01000000
62	3E	# 1 H sync offset (”46”)	2E	00101110
63	3F	# 1 H sync pulse width (”30”)	1E	00011110
64	40	# 1 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
66	42	# 1 H image size (“293 mm“)	25	00100101
67	43	# 1 V image size (“165 mm“)	A5	10100101
68	44	# 1 H image size : V image size	10	00010000
69	45	# 1 H boarder (”0”)	00	00000000
70	46	# 1 V boarder (”0”)	00	00000000
71	47	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
72	48	Detailed timing description # 2 Pixel clock (“92.52MHz”, According to VESA CVT Rev1.4)	24	00100100
73	49	# 2 Pixel clock (hex LSB first)	24	00100100
74	4A	# 2 H active (“1920”)	80	10000000
75	4B	# 2 H blank (“160”)	A0	10100000
76	4C	# 2 H active : H blank (“1920 :160”)	70	01110000
77	4D	# 2 V active (”1080”)	38	00111000
78	4E	# 2 V blank (”32”)	20	00100000
79	4F	# 2 V active : V blank (”1080 :32”)	40	01000000
80	50	# 2 H sync offset (”46”)	2E	00101110
81	51	# 2 H sync pulse width (”30”)	1E	00011110
82	52	# 2 V sync offset : V sync pulse width (”2 : 4”)	24	00100100
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width (”46: 30 : 2 : 4”)	00	00000000
84	54	# 2 H image size (“293 mm“)	25	00100101
85	55	# 2 V image size (“165 mm“)	A5	10100101

86	56	# 2 H image size : V image size	10	00010000
87	57	# 2 H boarder ("0")	00	00000000
88	58	# 2 V boarder ("0")	00	00000000
89	59	Non-interlaced, Normal Display, Digital separate, Positive Hsync, Negative Vsync	1A	00011010
90	5A	Flag	00	00000000
91	5B	Flag	00	00000000
92	5C	Flag	00	00000000
93	5D	Data Type Tag: Alphanumeric Data String (ASCII)	FE	11111110
94	5E	Flag	00	00000000
95	5F	Dell P/N 1st Character "V"	56	01010110
96	60	Dell P/N 2nd Character "K"	4B	01001011
97	61	Dell P/N 3rd Character "W"	57	01010111
98	62	Dell P/N 4th Character "J"	4A	01001010
99	63	Dell P/N 5th Character "C"	43	01000011
100	64	EDID Revision	80	10000000
101	65	Manufacturer P/N "1"	31	00110001
102	66	Manufacturer P/N "3"	33	00110011
103	67	Manufacturer P/N "3"	33	00110011
104	68	Manufacturer P/N "H"	48	01001000
105	69	Manufacturer P/N "S"	53	01010011
106	6A	Manufacturer P/N "E"	45	01000101
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag: Manufacturer Specified Data 00	00	00000000
112	70	Flag	00	00000000
113	71	Color Management	0A	00001010
114	72	Panel Type and Revision	41	01000001
115	73	Frame Rate	31	00110001
116	74	Light Controller Interface and Maximum Luminance	A3	10100011
117	75	Front Surface / Polarizer and Pixel Structure	00	00000000
118	76	Multi-Media Features	10	00010000
119	77	Multi-Media Features	00	00000000
120	78	Special Features	00	00000000
121	79	Special Feature	0A	00001010
122	7A	Special Features	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	No extension	00	00000000
127	7F	Checksum	20	00100000

10 .Inspection Specifications

The buyer (customer) shall inspect the modules within twenty calendar days since the delivery date (the "inspection period") at its own cost. The results of the inspection (acceptance or rejection) shall be recorded in writing, and a copy of this writing will be promptly sent to the seller.

The buyer may, under commercially reasonable reject procedures, reject an entire lot in the delivery involved if, within the inspection period, such samples of modules within such lot show an unacceptable number of defects in accordance with this incoming inspection standards, provided however that the buyer must notify the seller in writing of any such rejection promptly, and not later than within three business days of the end of the inspection period.

Should the buyer fail to notify the seller within the inspection period, the buyer's right to reject the modules shall be lapsed and the modules shall be deemed to have been accepted by the buyer.

11. Warranty

Inteltronic Inc. warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for one year from the date of purchase.

Inteltronic Inc. will be limited to replace or repair any of its module which is found and confirmed defective electrically or visually when inspected in accordance with Inteltronic Inc. general module inspection standard.

This warranty does not apply to any products which have been on customer’s production line, repaired or altered by persons other than repair personnel authorized by Inteltronic Inc., or which have been subject to misuse, abuse, accident or improper installation. Inteltronic Inc. assumes no liability under the terms of this warranty as a consequence of such events.

If an Inteltronic Inc. product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. In returning the modules, they must be properly packaged with original package; there should be detailed description of the failures or defect.

12. RMA

Products purchased through Inteltronic Inc. and under warranty may be returned for replacement. Contact support@inteltronicinc.com for RMA number and procedures

Office Locations

INTELTRONIC

Inteltronic Inc.
www.inteltronicinc.com
Office: 510-471-9900
Fax: 510-471-9901
Address: 29470 Union City Blvd
Union City, CA 94587

www.wahlee.com
Wah Lee Industrial Corp.
HSINCHU OFFICE
18F, No.8, Zihciang S. Rd., Jhubei,
Hsinchu 302, Taiwan, R.O.C.
Tel : 886-3-6205880
FAX: 886-3-6205833